REMARKS

Claim Rejections – 35 U.S.C. § 103

The Examiner has rejected claims 1-4 and 6-8 under 35 U.S.C §103(a) as being unpatentable over Lin (U.S. Patent 6,297,554) in view of Jun (U.S. Patent 5,900,072). Claims 5, 9, and 24 are rejected under 35 U.S.C §103(a) as being unpatentable over Lin in view of Jun and further in view of Cho et al. (U.S. Patent 6,140,252).

It is Applicant's understanding that the cited references fail to teach or render obvious Applicant's invention as claimed in claims 1-9 and 24.

With respect to independent claim 1, Applicant teaches and claims a process of lowering a parasitic capacitance between interconnect lines by forming a first dielectric layer and patterning the first dielectric layer such that a plurality of vertically oriented posts are formed, with each post having a top surface. The first dielectric layer has a dielectric constant. The process further comprises the formation of a second dielectric layer over and adjacent to the posts, where the second dielectric layer has a dielectric constant that is lower than the dielectric constant of the first dielectric layer. The above mentioned posts are formed to provide a mechanical reinforcement of the bulk of the inter-layer dielectric material. Finally, the process comprises polishing the second dielectric layer such that its top surface is substantially even with the top surfaces of the posts and the formation of an inlaid metal interconnection in the second dielectric layer.

On the other hand, Lin discloses forming a dielectric layer, where the structure of the dielectric layer comprises at least one trench with an aspect ratio greater than 3.5,

with an insulating layer in the trench and a void formed within the insulating layer (Col. 1, line 52 to 62).

Lin describes trenches which are different than the posts disclosed in the presently claimed invention. Lin does not teach posts as disclosed in the presently claimed invention. Applicant teaches and claims the use of posts 502 to provide structural reinforcement to the second layer dielectric during the polishing process. (Fig. 5) The posts are discrete features, having top surfaces such as posts 502a and 606. (Fig. 6) The trenches 72 taught by Lin must be of a specific size, having an aspect ratio greater than 3.5. Note Fig. 2 and Col. 3, lines 30 to 32 of Lin. Lin teaches that when the insulating layer is deposited over the trenches, said trenches having an aspect ratio greater than 3.5, the insulating layer forms overhangs on the dielectric layer around the top edges of the trenches. These overhangs close the trenches so as to form voids (Col. 3, line 45 to 50). The voids created by the overhangs effectively lower the dielectric constant of the dielectric layer. If one were to use a post as described and shown in Fig. 6 of the presently claimed invention for the purpose of Lin, overhangs would not be formed and, therefore, voids would not be formed in the manner described by Lin.

Jun discloses a first insulating layer 3 formed at regular intervals on substrate 10 and a second insulating layer 5 formed on the upper part of substrate 10, where insulating layer 3 has a groove 3a (See Fig. 1B), or a trench 6 (See Fig. 3D). Jun does not teach posts as disclosed in the presently claimed invention. Applicant teaches and claims the use of posts 502 to provide structural reinforcement to the second layer dielectric during the polishing process. (Fig. 5) The posts are discrete features, having top surfaces such as posts 502a and 606. (Fig. 6) Jun teaches an insulating layer comprising a groove 3a

or trench pattern 6 used for the purpose of planarizing the insulating layer without using the etch-back process of chemical mechanical polish. Note Fig 1B, Fig. 3D, and Col. 4, line 32 to 36 of Jun. Jun teaches that the pattern interval, or trench, between insulating layer 3 must be less than 10,000Å for the purpose of readily filling the insulating layer when it is deposited (Col. 3, line 27 to 33). Jun teaches a method of planarizing an insulating layer by forming a first insulating layer and a second insulating layer, as described in Col. 3, line 54 to 67 and Col. 4, line 1 to 15. The width of the trench in Jun ensures even coverage when the second insulating layer is deposited, such that the insulating layer is planarized without using a CMP process. Jun teaches not to planarize by chemical mechanical polishing (Col. 4, line 32 to 37). If one were to use a post as described and shown in Fig. 6 of the presently claimed invention for the purpose of Jun, planarization would not occur in the manner described by Jun, because the insulating layer would not be deposited with even coverage.

Thus, it is Applicant's understanding that both Lin and Jun fail to teach forming a plurality of vertically oriented posts. Additionally, both Lin and Jun fail to teach using said posts to provide mechanical reinforcement of the bulk of the inter-layer dielectric material.

Claims 2-4 and 6-8 are dependent upon independent claim 1. Thus, for at least the same reasons advanced above with respect to independent claim 1, Applicant respectfully submits that neither Lin nor Jun, independently or in combination, render these dependent claims obvious.

Claims 5 and 9 are dependent upon independent claim 1. Thus, for at least the same reasons advanced above with respect to independent claim 1, Applicant respectfully

submits that neither Lin, Jun, nor Cho, independently or in combination, render these dependent claims obvious.

With respect to independent claim 24, Applicant teaches and claims the formation of the inlaid metal interconnection in the second dielectric layer taking place after the CMP process. In Lin, a planarization process, such as chemical mechanical polishing (CMP), is performed to remove the copper layer 84 down to the surface of the insulating layer 82 so as to form the copper wiring lines 91, 92, 93 (See Fig. 7). The CMP process of Lin is performed after the copper damascene interconnects are formed, and is the last step in the process of forming a structure of a dielectric layer between two adjacent copper wiring lines (Fig. 1 – 8). Lin does not teach performing the CMP process on the dielectric layer prior to forming the metal damascene interconnections. Lin teaches performing the CMP process after the metal damascene interconnections are formed. Therefore, in Lin, the formation of inlaid metal interconnection does not take place after CMP of the dielectric layer as it takes place in the present invention.

Furthermore, Jun teaches a method for planarizing an insulating layer without using such an etch-back process of a chemical mechanical polish (CMP) (Col. 4, line 32 to 33).

Finally, Cho lacks at least the elements missing from Lin and Jun.

As such, it is Applicant's understanding that Lin, Jun, and Cho, taken alone or in combination, do not teach or render obvious Applicant's invention as claimed in claims 1-9 and 24.

Applicant respectfully requests the removal of the 35 U.S.C. 103(a) rejection of claims 1-9 and 24 and seeks an early allowance of these claims.

If there are any additional charges, please charge Deposit Account No 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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Michael A. Bernadicou
Reg. No. 35,934

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

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IN THE CLAIMS

24. (Amended) A process, comprising:

depositing a silicon nitride layer on a wafer;

depositing an insulating layer over the silicon nitride layer, wherein the insulating layer has a dielectric constant;

patterning the insulating layer such that a plurality of structures are formed, the structures each having a top surface;

depositing a porous dielectric material over and adjacent to the structures, the porous dielectric material having a void fraction, wherein the porous dielectric material substantially fills out the area adjacent to said structures and wherein the porous dielectric material has a dielectric constant, said dielectric constant of the insulating layer being higher than the dielectric constant of the porous dielectric material;

wherein said plurality of structures formed in the insulating layer provides mechanical reinforcement of the porous dielectric material which makes up the bulk of an inter-layer dielectric material;

polishing the porous dielectric material such that a top surface thereof is substantially even with the top surfaces of the structures;

[treating the porous dielectric material such that its void fraction is increased;] and

after polishing said porous dielectric material, forming an inlaid metal interconnection in the porous dielectric material.

25. (New) The process of Claim 24, further comprising treating the porous dielectric material such that its void fraction is increased.